## AMENDMENTS TO THE CLAIMS

**1-20. (canceled)**

**21. (new)** An image sensor comprising:

a sensor unit having a plurality of pixels;

a first scanning circuit for normal scanning, having a dynamic logic circuit for outputting one or more first selection signals for selecting pixels from among said plurality of pixels in said sensor unit;

a second scanning circuit for use as an electric shutter, having a dynamic logic circuit for outputting one or more second selection signals for selecting pixels from among said plurality of pixels in said sensor unit; and

one or more selection circuits, each configured to receive a first selection signal from among said one or more first selection signals and a second selection signal from among said one or more second selection signals, each selection circuit comprising:

a first bootstrap circuit configured to hold the received first selection signal, and to output a first AND signal obtained by performing a logical AND between the held first selection signal and a first drive signal, thereby specifying a timing to output the first AND signal; and

a second bootstrap circuit configured to hold the received second selection signal, and to output a second AND signal obtained by performing a logical AND between the held second selection signal and a second drive signal, thereby specifying a timing to output the second AND signal,

wherein each selection circuit of said one or more selection circuits outputs the first AND signal and the second AND signal to said sensor unit.

**22. (new)** A camera comprising:

a housing; and

the image sensor according to claim 21.

**23.** **(new)** The image sensor according to Claim 21,

wherein each first bootstrap circuit includes:

a first switch connected to a selection signal line from said first scanning circuit;

a first boosting transistor for holding the received first selection signal in a gate capacitor, said first boosting transistor having a drain, a source, and a gate; and

a first capacitative element for boosting a gate voltage in said first boosting transistor,

wherein each second bootstrap circuit includes:

a second switch connected to a selection signal line from said second scanning circuit;

a second boosting transistor for holding the received second selection signal in a gate capacitor, said second boosting transistor having a drain, a source, and a gate; and

a second capacitative element for boosting a gate voltage in said second boosting transistor,

wherein said first boosting transistor in each first bootstrap circuit outputs the first AND signal from one of said drain and said source of said first boosting transistor by an input of the first drive signal to the other of said drain and said source of said first boosting transistor,

wherein said second boosting transistor in each second bootstrap circuit outputs the second AND signal from one of said drain and said source of said second boosting transistor by an input of the second drive signal to the other of said drain and said source of said second boosting transistor, and

wherein, in each selection circuit, said one of said drain and said source of said first boosting transistor is connected to said one of said drain and said source of said second boosting transistor to output the first AND signal and the second AND signal to said sensor unit.

**24.** **(new)** The image sensor according to claim 23,

wherein, in each selection circuit, said first capacitative element is connected between either said drain or said source of said first boosting transistor and said gate of said first boosting

transistor, and

wherein, in each selection circuit, said second capacitative element is connected between either said drain or said source of said second boosting transistor and said gate of said second boosting transistor.

**25. (new)** The image sensor according to Claim 23,

wherein, in each selection circuit, at least one of said first capacitative element and said second capacitative element is a gate capacitor of an enhancement-type transistor having a drain and a source, and said drain and said source are short-circuited.

**26. (new)** The image sensor according to Claim 23,

wherein, in each selection circuit, said first switch transmits the received first selection signal to said gate of said first boosting transistor when said first switch is turned on, and said second switch transmits the received second selection signal to said gate of said second boosting transistor when said second switch is turned on, and

wherein, in each selection circuit, at least one of said first switch and said second switch transmits at a time when one horizontal scanning period shifts to another horizontal scanning period.

**27. (new)** The image sensor according to Claim 23,

wherein, in each selection circuit, at least one of said first switch and said second switch is a switching transistor, and

wherein, in each selection circuit, a threshold of a gate voltage to turn on said switching transistor is lower than a threshold of a gate voltage to turn on a respective one of said first boosting transistor and said second boosting transistor.

**28. (new)** The image sensor according to Claim 23,

wherein at least one first selection signal of the one or more first selection signals is at a high level during a portion of a horizontal scanning period in which the at least one first selection

signal is held, and

wherein at least one second selection signal of the one or more second selection signals is at a high level during a portion of a horizontal scanning period in which the at least one second selection signal is held.

**29. (new)** The image sensor according to Claim 28,

wherein, in each selection circuit, at least one of said first capacitative element and said second capacitative element is a gate capacitor of an enhancement-type transistor having a drain and a source, and said drain and said source are short-circuited.

**30. (new)** The image sensor according to Claim 28,

wherein at least one of the received first selection signal and the received second selection signal is a pulse having an arbitrary width, and the pulse is output using a drive pulse having the arbitrary width.

**31. (new)** The image sensor according to Claim 28,

wherein, in each selection circuit, said first switch transmits the received first selection signal to said gate of said first boosting transistor when said first switch is turned on, and said second switch transmits the received second selection signal to said gate of said second boosting transistor when said second switch is turned on, and

wherein, in each selection circuit, at least one of said first switch and said second switch transmits at a time when one horizontal scanning period shifts to another horizontal scanning period.

**32. (new)** The image sensor according to Claim 28,

wherein, in each selection circuit, at least one of said first switch and said second switch is a switching transistor, and

wherein a threshold of a gate voltage to turn on said switching transistor is lower than a threshold of a gate voltage to turn on a respective one of said first boosting transistor and said

second boosting transistor.

**33. (new)** The image sensor according to Claim 28,

wherein said first scanning circuit outputs the one or more first selection signals at a high level by use of a drive pulse that is at a high level, and

wherein said second scanning circuit outputs the one or more second selection signals at a high level by use of a drive pulse that is at a high level.

**34. (new)** The image sensor according to Claim 33,

wherein, in each selection circuit, at least one of said first switch and said second switch is a switching transistor, and

wherein a threshold of a gate voltage to turn on said switching transistor is lower than a threshold of a gate voltage to turn on a respective one of said first boosting transistor and said second boosting transistor.

**35. (new)** The image sensor according to Claim 34,

wherein each switching transistor transmits at least one of the received first selection signal and the received second selection signal to said gate of a respective one of said first boosting transistor and said second boosting transistor when said switch is turned on at a time when one horizontal scanning period shifts to another horizontal scanning period.

**36. (new)** A driving method for use with an image sensor,

wherein the image sensor comprises:

a sensor unit having a plurality of pixels;

a first scanning circuit for normal scanning, having a dynamic logic circuit for outputting one or more first selection signals for selecting pixels from among said plurality of pixels in said sensor unit;

a second scanning circuit for use as an electric shutter, having a dynamic logic circuit for outputting one or more second selection signals for selecting pixels from among said plurality of

pixels in said sensor unit; and

one or more selection circuits, each configured to receive a first selection signal from among said one or more first selection signals and a second selection signal from among said one or more second selection signals, each selection circuit comprising:

a first bootstrap circuit configured to hold the received first selection signal, and to output a first AND signal obtained by performing a logical AND between the held first selection signal and a first drive signal, thereby specifying a timing to output the first AND signal; and

a second bootstrap circuit configured to hold the received second selection signal, and to output a second AND signal obtained by performing a logical AND between the held second selection signal and a second drive signal, thereby specifying a timing to output the second AND signal,

wherein each selection circuit of said one or more selection circuits outputs the first AND signal and the second AND signal to said sensor unit,

the method comprising:

a holding step of holding, in the second bootstrap circuit of a selection circuit of the one or more selection circuits, the received second selection signal outputted from the second scanning circuit during one horizontal scanning period;

an output step of outputting, to the sensor unit of the selection circuit of the one or more selection circuits, an AND signal obtained by performing a logical AND between the received second selection signal held in the second bootstrap circuit and a second drive signal that specifies a timing to output the AND signal to the sensor unit,

a holding step of holding, in the first bootstrap circuit of the selection circuit of the one or more selection circuits, the received first selection signal outputted from the first scanning circuit during one horizontal scanning period; and

an output step of outputting, to the sensor unit of the selection circuit of the one or more selection circuits, an AND signal obtained by performing a logical AND between the received first selection signal held in the first bootstrap circuit and a first drive signal that specifies a timing to output the AND signal to the sensor unit.